IN THE CLAIMS

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

1. (Currently Amended) Method of emulating a design under test associated with a test environment, the method comprising:

generating, in a first phase, a first file ~~for configuring~~ representative of a synthesizable portion of the test environment, and

generating in a second phase, a second file ~~for configuring~~ representative of at least a part of the design under test,

delivering the first configuration file to a first reconfigurable hardware part forming a reconfigurable test bench so as to ~~configure the test bench~~ emulate the synthesizable portion of the test environment,

delivering the second configuration file to a second reconfigurable hardware part so as to ~~configure an emulator of~~ emulate the design under test, and

performing stimulation, using the reconfigurable test bench, ~~of the emulator of the device under test~~ to produce emulation test results,

wherein the first and second reconfigurable [[two]] hardware parts are distinct and mutually connected.

2. (Currently Amended) Method according to claim 1, wherein the first phase comprises:

producing a logic circuit comprising a network of logic gates, the logic circuit being representative of the synthesizable portion of the test environment and compilation directives, and

compiling the logic circuit in accordance with ~~the compilation~~ said directives, so as to obtain the first configuration file.

3. (Previously Presented) Method according to claim 2, wherein the test environment comprises a collection of drivers and of monitors, and the production of the logic circuit comprises the formation of hardware blocks in the form of networks of logic gates, these hardware blocks representing: interfaces of drivers/monitors of software stimulation, interfaces of drivers/monitors of real hardware stimulation, and drivers/monitors of emulated hardware stimulation, blocks for calculations of hardware triggers, and a block for interfacing with the emulator of the design under test.

4. (Previously Presented) Method according to claim 3, wherein the formation of the hardware blocks is effected on the basis of statically defined networks of gates or of networks of gates which are generated dynamically by a software module.

5. (Previously Presented) Method according to any one of claims 1 to 4, wherein the first phase and the second phase are performed in parallel.

6. (Previously Presented) Method according to any one of claims 1 to 4, wherein the first phase and the second phase are performed sequentially.

7. (Previously Presented) Method according to claim 6, wherein the first phase is performed before or after the second phase.

8. (Previously Presented) Method according to claim 3, wherein

when the first phase is performed after the second phase, the production of the logic circuit uses as input parameters a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, and

when the second phase is performed after the first phase, the production of the logic circuit uses as input parameters a description of the interface of the design under test and supplies as output a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, the output description being used as a constraint parameter for the second phase.

9. (Currently Amended) Emulation system for emulating a design under test associated with a test environment, the system comprising:

a host computer,

a reconfigurable hardware test bench connected to the host computer and operable to emulate ~~at least a part~~ a synthesizable portion of the test environment,

a reconfigurable hardware emulator, connected to and distinct from the test bench, and operable to emulate ~~at least a part of~~ the design under test,

first generating means operable to generate a first file ~~for configuring~~ representative of the test environment, and

second generating means operable to generate a second file ~~for configuring~~ representative of the design under test.

10. (Previously Presented) System according to claim 9, wherein the reconfigurable test bench comprises a fixed part and at least one reconfigurable interface circuit embodying the emulated part of the test environment.

11. (Previously Presented) System according to claim 10, wherein the fixed part comprises at least one control circuit and one circuit for interfacing with the host computer, and the reconfigurable interface circuit comprises interfaces of drivers/monitors of software stimulation which are operable to establish communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

12. (Previously Presented) System according to claim 11, wherein the fixed part furthermore comprises hardware drivers/monitors, and the reconfigurable circuit comprises interfaces with the hardware drivers/monitors.

13. (Previously Presented) System according to any one of claims 9 to 12, wherein the fixed part comprises a circuit for interfacing with a target device.

14. (Previously Presented) System according to claim 9, wherein the

fixed part comprises a control part of a hardware logic analyser whose state evolves as a function of the hardware triggers.

15. (Previously Presented) System according to claim 9, wherein the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals synchronizing the emulator of the design under test and certain at least of the hardware means of the test bench, the reconfigurable test bench further comprising clock retrocontrol means operable to, in response to at least one wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal, of temporarily disable certain of the other secondary clock signals with different frequencies from that of the first secondary clock signal.

16. (Previously Presented) System according to claim 9, wherein the test bench and the emulator are embodied on an electronic card external to the host computer and connected to a mother card of the host computer.

17. (Previously Presented) System according to claim 9, wherein the reconfigurable test bench is embodied on a first electronic card external to the host computer and connected to a mother card of the host computer, and the emulator of the design under test is embodied on one or more other cards external to the host computer and connected to the first electronic card.

18. (Previously Presented) System according to claim 17, wherein the circuit for interfacing with the target device is integrated into the first electronic card.

19. (Previously Presented) System according to any one of claims 10 to 12, wherein the test bench and the emulator are embodied on an internal electronic card (CINT) incorporated into the host computer.

20. (Previously Presented) System according to claim 13, wherein the circuit for interfacing with the target device is embodied on an external electronic card outside the host computer, and configured to be connected to the internal electronic card.

21. (Currently Amended) An apparatus in the form of an electronic card configured to be connected to the mother card of a host computer, the electronic card comprising:

a reconfigurable hardware test bench operable to emulate ~~at least a part~~ a synthesizable portion of a test environment associated with a design under test, and

a reconfigurable hardware emulator, distinct from the test bench, connected to the reconfigurable test bench and operable to emulate ~~at least a part of~~ the design under test.

22. (Previously Presented) The apparatus according to claim 21, wherein the reconfigurable test bench comprises a fixed part and at least one reconfigurable circuit operable to embody the emulated part of the test environment.

23. (Previously Presented) The apparatus according to claim 22, wherein the fixed part comprises at least one control circuit and one circuit for interfacing with the host computer, and the reconfigurable circuit comprises interfaces of drivers/monitors of software stimulation which are operable to establish communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

24. (Previously Presented) The apparatus according to claim 23, wherein the fixed part furthermore comprises hardware drivers/monitors, and the reconfigurable circuit comprises interfaces with the hardware drivers/monitors.

25. (Previously Presented) The apparatus according to any one of claims 21 to 24, wherein the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals of different frequencies, the reconfigurable test bench further comprising clock retrocontrol means operable to, in response to a wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal, of temporarily disable the secondary clock signals with different frequencies from that of the first secondary clock signal.